SATHYABAMA
INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)
Accredited with 'A' grade by NAAC
Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai - 600 119.

Department of Mechatronics Engineering

School of Mechanical Engineering

Minutes of Board of Studies Meeting held on 15-12-2018 (Saturday)

Meet Time: 11.00 am to 1.00 pm

The meeting started with the welcome address delivered by Dr. S. Prakash, Professor and Dean (Session Chair). He introduced the courses offered to the mechatronics Engineering students to the BOS panel members. The following are the BOS members were present during the Mechatronics Engineering BOS meeting.

Sl. No.	Name	Designation	Institution	Role
1	Dr. S. Prakash	Professor and Dean	Sathyabama Institute of Science & Technology	Chair person
2	Dr.L.Vijayaraghavan	Professor	IIT Madras, Chennai	BoS Member (External)
3	Dr.N.GaneshKumar	Associate Professor	PSG Tech, Coimbatore	BoS Member (External)
4	Dr. S. Sivasaravanan	Associate Professor	Sathyabama Institute of Science & Technology	Member
5	Mrs. M Sangeetha	Assistant Professor	Sathyabama Institute of Science & Technology	Member
6	Mr. J. R. Deepak	Assistant Professor	Sathyabama Institute of Science & Technology	Member
7	Dr. J. Lilly Mercy	Assistant Professor	Sathyabama Institute of Science & Technology	Member
8	Mr. V. Jayaprakash	Assistant Professor	Sathyabama Institute of Science & Technology	Member
9	Mr. J. Senthil Kumar	Assistant Professor	Sathyabama Institute of Science & Technology	Member
10	Mr. M Vigneshwar	Student	Sathyabama Institute of Science & Technology	Member
11	Mr Aman Dinodya	Student	Sathyabama Institute of Science & Technology	Member

Agenda for the BOS Meeting:

Subject Matter Expert Review and Comments on the syllabus

The BOS meeting has been convened on 15-12-2018 to review the new courses for the newly proposed program B.E Mechatronics engineering which was implemented for the Academic Year 2018-19.

- Dr. S. Sivasaravanan proposed a new course entitled **Digital Electronics** based on the futuristic requirements for the students. The curriculum consists of various engineering discipline to promote inter disciplinary innovate thinking in students. The students will be able to design various combinational, sequential circuits and develop digital system designs using. The students will create simulation models using VHDL software. The backdrop in introducing such courses is to promote collaborative research among the students leading to novel ideas in the field of digital electronics. The students will be able to select the appropriate memory devices and develop digital circuits for real time applications.

- Dr. N. Ganesh Kumar, Associate Professor from PSG Tech welcomed the idea of introducing **Digital Electronics** course in the first year (second semester) saying that Sathyabama Institute of science and technology would be the pioneer in introducing **Digital Electronics** in the Mechatronics curriculum**.**

- Dr. L. Vijayaraghavan, Professor from IIT Madras, Chennai and Dr. N. Ganesh Kumar, Associate Professor from PSG Tech (External BOS members) reviewed the course. The Board members appreciated the inclusion of the new course **Digital Electronics** in 2018 Regulation.

- **New Course Entitled Digital Electronics**

SMR1101 DIGITAL ELECTRONICS
L T P Credits Total Marks
3 0 0 3 100

COURSE OBJECTIVES
On completion of this course the student will recognize

- Acquire knowledge about the Digital Design
- Acquire knowledge about Classifications and Characteristics of Memory
- Acquire knowledge about Simulation

UNIT 1 FUNDAMENTALS OF DIGITAL DESIGN 9Hrs.
Logic Gates: Basic gates, Universal gates, Sum of products and products of sum, minimization with Karnaugh Map (upto four variables) and realization. Logic Families: Types of logic families (TTL and CMOS), characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in), transfer characteristics of TTL NAND, Interfacing CMOS to TTL and TTL to CMOS Combinational Circuits using basic gates as well as MSI devices: Half adder, Full adder, Half Subtractor, Full Subtractor, multiplexer, demultiplexer, decoder, Comparator (Multiplexer and demultiplexer gate level up to 4:1). MSI devices IC7483, IC74151, IC74138, IC7485.

UNIT 2 ELEMENTS OF SEQUENTIAL LOGIC DESIGN 9 Hrs.
2.1 Sequential Logic: Latches and Flip-Flops, Conversion of flip flops (timing considerations and metastability are not expected) 2.2 Counters: Asynchronous, Synchronous Counters, Up Down Counters, Mod Counters, Ring Counters Shift Registers, Universal Shift Register

UNIT 3 SEQUENTIAL LOGIC DESIGN 9 Hrs.
Mealy and Moore Machines, clocked synchronous state machine analysis, State reduction techniques and state assignment, Clocked synchronous state machine design. (Complex word problems like traffic light controller etc. are not expected) MSI counters (7490, 74163, 74169) and applications, MSI Shift registers (74194) and their applications.

UNIT 4 MEMORIES AND PROGRAMMABLE LOGIC DEVICES 9 Hrs.
Classification and characteristics of memory: SRAM, DRAM, ROM, PROM, EPROM and FLASH memories 4.2 Concepts of PAL and PLA. Architecture of CPLD and FPGA, Xilinx XC 9500 CPLD Series and Xilinx XC 4000 FPGA Series.

UNIT 5 SIMULATION 9 Hrs.
Functional Simulation, Timing simulation, Logic Synthesis, RTL, VHDL: Data types, Structural Modeling using VHDL, Implementation of basic combinational and sequential Circuits

Max. 45 Hours

COURSE OUTCOME
On completion of the course, student will be able to
CO1 - Examine the structure of number systems and perform the conversion among different number systems
CO2 - Illustrate reduction of logical expressions using boolean algebra, k-map and tabulation method and implement the functions using logic gates
CO3 - Realize combinational circuits for given application
CO4 - Understand the working mechanism and design guidelines of different combinational, sequential circuits and their role in the digital system design.
CO5 - Understand the concepts of simulation model, structural modelling using VHDL
CO6 - Assess the nomenclature and technology in the area of memory devices and apply the memory devices in different types of digital circuits for real world application.

TEXT / REFERENCE BOOKS

1. William I. Fletcher, 'An Engineering Approach to Digital Design', PHI.
2. B. Holdsworth and R. C. Woods, 'Digital Logic Design', Newnes, 4th Edition
3. Morris Mano, Digital Design, Pearson Education, Asia 2002.
4. John F. Wakerley, Digital Design Principles And Practices, third Edition Updated, Pearson Education, Singapore, 2002
5. Anil K. Maini, Digital Electronics, Principles, Devices and Applications, Wiley
6. Stephen Brown and Zvonko Vranesic, Fundamentals of digital logic design with VHDL, McGraw Hill, 2nd Edition

END SEMESTER EXAM QUESTION PAPER PATTERN

Max. Marks : 100 Exam Duration : 3 Hrs.

PART A : 2 Questions from each unit, each carrying 2 marks 20 Marks

PART B : 2 Questions from each unit with internal choice, each carrying 16 marks 80 Marks

- Signature of BOS members

Sl. No.	Name	Signature
1	Dr. S. Prakash	
2	Dr.L.Vijayaraghavan	
3	Dr.N.Ganesh Kumar	
4	Dr. B. Kanimozhi	
5	Dr. S. Sivasaravanan	
6	Dr. M Sangeetha	
7	Dr. J. R. Deepak	
8	Dr.J. Lilly Mercy	
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